Attorney Docket No. 5051-531DV PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Divisional of: Zhibo Zhang
Application Serial No.: To Be Assigned
Filed: Concurrently Herewith
For: VERTICAL FIELD EFFECT TRANSISTORS INCLUDING CONFORMAL MONOCRYSTALLLINE SILICON LAYER ON TRENCH SIDEWALL

October 2, 2003

Mail Stop PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on form PTO-1449. Items 1-25 listed on the PTO-1449 were cited in parent application Serial No. 10/007,895, filed November 6, 2001. Since the benefit of this application is claimed under 35 U.S.C. §120, no copies need to be furnished in accordance with 37 C.F.R. §1.98(d); however, copies will be furnished on request. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. §1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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Susan E. Freedman
Date of Signature: October 2, 2003

Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 5051-531DV	Serial No. To Be Assigned
LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)	Applicants: Zhibo Zhang	
	Filing Date: To Be Assigned	GAU:

U.S. PATENT DOCUMENTS

Examiner Initials		Document No.	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	6,420,751	07/16/2002	Maeda et al.	257	302	
	2	6,049,106	04/11/00	Forbes	257	329	
	3	5,739,057	04/14/98	Tiwari et al.	438	172	
	4	5,757,038	05/26/98	Tiwari et al.	257	192	
	5	5,106,778	04/21/92	Hollis et al.	437	90	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	6	Yeo et al., *Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET With a SiGe/Si Heterostructure Channel*, IEEE Electron Device Letters, Vol. 21, No. 4, April 2000, pp. 161-163
	7	*International Technology Roadmap for Semiconductors, 1999 Edition*
	8	Lee et al., *Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy*, International Electron Devices Meeting, 1999, pp. 71-74
	9	Hergenrother et al., *The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET With Lithography-Independent Gate Length*, International Electron Devices Meeting, 1999, pp. 75-78
	10	Yang et al., *25-nm p-Channel Vertical MOSFET's With SiGeC Source-Drains*, IEEE Electron Device Letters, Vol. 20, No. 6, June 1999, pp. 301-303
	11	Subramanian et al., *Low-Leakage Germanium-Seeded Laterally-Crystallized Single-Gran 100-nm TFT's for Vertical Integration Applications*, IEEE Electron Device Letters, Vol. 20, NO. 7, July 1999, pp. 341-343
	12	Choi et al., *Ultra-Thin Body SOI MOSFET for Deep-Sub-Tenth Micro Era*, International Electron Devices Meeting, 1999, pp. 919-921
	13	Wong, *Vertical Slab*, IEDM Short Course, 1999, p. 30
	14	Jin et al., *Nickel Induced Crystallization of Amorphous Silicon Thin Films*, Journal of Applied Physics, Vol. 84, No. 1, July 1, 1998, pp. 194-200
	15	Hisamoto et al., *A Folded-Channel MOSFET for Deep-Sub Tenth Micron Era*, International Electron Devices Meeting, 1998, pp. 1032-1034
	16	Wong et al., *Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation*, International Electron Devices Meeting, 1998, pp. 407-410
	17	Yu et al., *"Ultra-Thin-Body Silicon-on-Insulator MOSFET's for Terabit-Scale Integration"*; 1997 International Semiconductor Device Research Symposium, University of Virginia, Charlottesville, VA, Dec. 11-13, 1997, p. 623
	18	Leobandung et al., *Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors With a Significant Reduction of Short Channel Effects*, J. Vac. Sci. Technol. B, Vol. 5, No. 6, Nov/Dec 1997, pp. 2791-2794
	19	Taur et al., *CMOS Scaling Into the Nanometer Regime*, Proceedings of the IEEE, Vol. 85, No. 4, April 1997, pp. 486-504
	20	Auth et al., *Scaling Theory for Cylindrical Fully-Depleted, Surrounding-Gate MOSFET's*, IEEE Electron Device Letters, Vol. 18, No. 2, February 1997, pp. 74-76
	21	Risch et al., *Vertical MOS Transistors With 70 nm Channel Length*, IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498
	22	Wann et al., *A Comparative Study of Advanced MOSFET Concepts*, IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1742-1753
	23	Tanaka et al., *Ultrafast Operation of V_{th}-Adjusted p^+-n^+ Double-Gate SOI MOSFET's*, IEEE Electron Device Letters, Vol. 15, No. 10, October 1994, pp. 386-388
	24	Colinge et al., *Silicon-on-Insulator "Gate-All-Around Device"*, International Electron Devices Meeting, 1990, pp. 595-598
	25	Takato et al., *High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs*, International Electron Devices Meeting, 1988, pp. 222-225

Examiner: _____ Date Considered: _____

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.